REMARKS

Claims 21-23, 25, and 34-41 are pending and rejected in the present application. Claims 21, 34 and 40 are amended hereby.

Applicants have carefully reviewed the prosecution history, specification and claims in an attempt to address all outstanding objections and rejections. Based on that review, Applicants have amended the present Specification as more particularly described in the "In the Specification" section hereinabove. Further, Applicants have amended claims 24 and 40 to address the 35 U.S.C. §112, second paragraph, issues that were generally referred to by the Examiner in the Advisory Action mailed 24 July 2003. Applicants submit that the Specification and claims are now in allowable form. Accordingly, Applicants respectfully request withdrawal of all objections and the rejections made under 35 U.S.C. §112, second paragraph.

In the Final Office Action, the pending claims were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,298,780 (Harada) in view of U.S. Patent No. 5,877,527 (Okabe, et al). In the event Applicants Response to Final was not persuasive, Applicants respectfully traverse the rejection hereinafter.

To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).* Applicants submit that the cited references

fail to disclose or suggest all the limitations of claim 21, and that therefore a *prima facie* case of obviousness has not been established.

Harada discloses a process for fabricating a semiconductor device that includes grooves 40 (*Fig. 8*) having a gate oxide film or layer 13 formed on the sidewalls and floor thereof. The grooves 40 are fully filled with a thick conductive film 4a such as doped polysilicon. (*column 5, lines 10-12*). Film 4a is etched back (*Fig. 9*), and the remaining upper portions thereof are oxidized to form oxide films 4b within grooves 40. (*Fig. 10, column 5, lines 20-23*). The thickness of the oxide films 4b determines the depth of source regions 5. The oxide films 4b and parts of the oxide films 13 in contact therewith are removed to expose the upper portions of grooves 40 (or recesses 41). (*Fig. 11, column 5, lines 20-23*). Heat treatment diffuses the impurities within oxide film 15a into body 3 so that N+ type source regions 5 are formed. (*Fig. 12, column 5, lines 34-37*). The impurity concentration of source regions 5 decreases away from grooves 40. (*column 5, lines 47-48*).

In contrast, claim 21 recites in part "filling each of said gate trenches to a selected level substantially below the upper surface of said upper level [of the substrate] with a conductive gate material". (*Emphasis Added*). Applicants submit that such a limitation is not disclosed or suggested by the cited references, alone or in combination.

The Examiner asserts that Harada discloses filling each of the gate trenches to a selected level substantially below the upper surface of the upper level of the substrate (*page 5, paragraph 13 of the Final Office Action mailed 25 April 2003*). However, Harada contradicts that assertion.

Harada performs different steps than are performed by the method of the present invention. Harada fills the gate trenches with a conductive material, an upper portion of which is then oxidized. Source regions are then formed by heat diffusion of dopants from the oxidized gate material into the device body. In contrast, the present invention only partially fills the gate trenches with conductive material, which is then covered with dielectric material, and source regions are formed by ion implantation to be coplanar with the level of the gate conductive material. Because the method of Harada forms source regions by diffusion, the source regions extend below the level of the gate conductive material. Unlike the method of the present invention, the method of Harada can not form source regions that are coplanar with the top or upper level of the gate conductive material.

Harada teaches that the grooves are completely filled with a thick conductive film that also covers the top surface of the substrate. The film is then removed from the top surface of the substrate by etching which leaves conductive film filling the grooves. The gate trenches or grooves of Harada are completely filled with conductive film. The gate trenches or grooves of Harada

are not filled to a selected level, nor are they filled to a selected level that is substantially below the upper surface of the upper level of the substrate. Thus, Harada fails to disclose or suggest filling each of the gate trenches to a selected level substantially below the upper surface of said the level of the substrate with a conductive gate material, as recited in part by claim 21.

Claim 21 also recites in part "forming an isolation layer of dielectric material on the upper surface of said upper layer and over said dielectric material covering said sidewalls within said gate trench". (*Emphasis Added*). Applicants submit that such limitations are not disclosed or suggested by the cited references, alone or in combination.

Harada completely removes the dielectric material that covers the trench sidewalls above the conductive gate material. (*see any of Figs. 11-14*). Further, Harada teaches that excessive etching can be used to remove gate oxide films exposed in the gate trenches. (*column 6, lines 2-5*). Therefore, the oxide layers subsequently deposited into the gate grooves or trenches is in direct contact with the uninsulated sidewalls of the trenches and, thus, with body region 3. Without that direct contact between the oxide layer and the body region, the diffusion of the N+ dopants to form the source regions, as described above, would be precluded. Thus, Harada fails to disclose or suggest forming an isolation layer of dielectric material on the upper surface of said upper layer and over said

dielectric material covering said sidewalls within said gate trench, as recited in part by claim 21.

Claim 21 also recites in part "forming a plurality of heavily doped source regions . . . extending to a selected depth from the upper surface of said upper layer . . . [that] is substantially coplanar with the level of the conductive gate material in the trench". (*Emphasis Added*). Applicants submit that such a limitation is not disclosed or suggested by the cited references, alone or in combination.

The source regions of Harada extend to a level substantially below the level of conductive gate material within the gate grooves. (*see, e.g., Fig. 12*). The bottoms of the source regions of Harada are not coplanar with the top of the conductive gate material. Thus, Harada fails to disclose or suggest forming a plurality of heavily doped source regions that extend to a selected depth that is substantially coplanar with the level of the conductive gate material in the trench, as recited in part by claim 21.

Thus, in summary, Harada fails to disclose or suggest, alone or in combination with Okabe, et al., forming an isolation layer of dielectric material over the dielectric material covering the gate trench sidewalls, as recited in part by claim 21. Harada also fails to disclose or suggest, alone or in combination with Okabe, et al., forming source regions that extend to a selected depth that is

substantially coplanar with the level of the conductive gate material in the trench, as recited in part by claim 21.

Since the cited references fail, alone or in combination, to recite all the limitations of claim 21, Applicants submit that a *prima facie* case of obviousness has not been established. Accordingly, Applicants respectfully request withdrawal of the rejection and allowance of claim 21 and claims 22-23, 25, and 24-39 depending therefrom.

Claim 40 was also rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,298,780 (Harada) in view of U.S. Patent No. 5,877,527 (Okabe, et al). In the event Applicants Response to Final was not persuasive, Applicants respectfully traverse the rejection hereinafter.

Claim 40 recites in part "filling each of said gate trenches to a selected level substantially below the upper surface of said upper level [of the substrate] with a conductive gate material" and "forming an isolation layer of dielectric material on the upper surface of said upper layer and over said dielectric material covering said sidewalls within said gate trench". (*Emphasis Added*). Thus, claim 40 recites in part subject matter that is substantially similar to the subject matter recited in part by claim 21. For the same reasons given above in regard to claim 21, Applicants submit that a *prima facie* case of obviousness has not been established in regard to claim 40. Accordingly, Applicants respectfully request

withdrawal of the rejection and allowance of claim 40 and claim 41 depending therefrom.

For all the foregoing reasons, Applicants submit that the pending claims are definite and do particularly point out and distinctly claim that which Applicants regard as the invention. Further, Applicants submit no combination of the cited references disclose or suggest the subject matter of the pending claims. The pending claims are therefore in allowable form and in condition for allowance. Accordingly, Applicants respectfully request withdrawal of all objections and rejections, and allowance of the claims.

The Examiner is invited to telephone the undersigned in regard to this Amendment and the above identified application.

Respectfully submitted,

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Date

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